AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (previously presented) An intercommunicating apparatus for transmitting a plurality of intercommunicating signals parallel to one another from a first processor unit to a second processor unit of a duplex processor apparatus, said intercommunicating apparatus comprising:

an output driver having

an input side connected to said first processor unit for receiving intercommunicating signals for said first processor and

an output side for transmitting said intercommunicating signals supplied from said first processor unit in the form of a serial signal having a redundancy data structure; and

an input driver having

an input side connected to said output side of said output driver to receive said serial signal having a redundancy data structure and

an output side connected to said second processor unit,

said input driver for receiving said serial signal transmitted from said output driver to reproduce said intercommunicating signals in the form of parallel signals and to

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supply the reproduced intercommunicating signals, from said output side, to said second processor unit.

2. (previously presented) An intercommunicating apparatus as claimed in Claim 1, wherein said output driver comprises a coding circuit for producing an error detecting code signal as said serial signal,

said input driver comprises a decoding circuit for decoding said error detecting code signal to detect an error on said error detecting code signal, said decoding circuit suspending supply of said reproduced intercommunicating signals to said second processor unit when said error is detected.

3. (previously presented) An intercommunicating apparatus as claimed in Claim 2, wherein said coding circuit comprises:

a redundancy bit producing circuit connected to said first processor unit for producing at least one redundancy bit on the basis of said intercommunicating signals, and

a multiplexing circuit connected to said redundancy bit producing circuit for multiplexing said intercommunicating signals and said redundancy bit(s) in a predetermined cycle to produce said serial signal,

said decoding circuit comprising:

a demultiplexing circuit connected to said multiplexing circuit for demultiplexing said serial signal into received intercommunicating signals and received redundancy bit(s),

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an error detecting circuit connected to said demultiplexing circuit for detecting an error on said received intercommunicating signals by the use of said received redundancy bit(s), and

a signal holding circuit connected to said error detecting circuit and said second processor unit for holding said received intercommunicating signals to supply said received intercommunicating signals as said reproduced intercommunicating signals to said second processor unit.

4. (original) An intercommunicating apparatus as claimed in Claim 3, wherein said error detecting circuit clears held content held in said signal holding circuit to suspend supply of said reproduced intercommunicating signals to the second processor unit when said error is detected.

5. (original) An intercommunicating apparatus as claimed in Claim 3, said redundancy bit producing circuit comprises a parity generating circuit for generating a parity bit as said redundancy bit.

6. (original) An intercommunicating apparatus as claimed in Claim 3, said redundancy bit producing circuit uses an error correction code or a cyclic redundancy check code to produce said redundancy bit(s).

7. (currently amended) An intercommunicating apparatus as claimed in Claim 3, said ~~cording~~ coding circuit further comprises a timing generating circuit connected to said

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multiplexing circuit for generating a timing signal to decide said predetermined cycle.

8. (original) An intercommunicating apparatus as claimed in Claim 3, said decoding circuit further comprises a timer circuit connected to demultiplexing circuit and said signal holding circuit for clearing held content held in said signal holding circuit to suspend supply of said reproduced intercommunicating signals to the second processor unit when said demultiplexing circuit does not receive said serial signal for a predetermined time period.

9. (original) An intercommunicating apparatus as claimed in claim 1, said intercommunicating apparatus further comprises:

an additional output driver connected to said second processor unit and having the same structure as said output driver for transmitting additional intercommunicating signals supplied from said second processor unit; and

an additional input driver connected to said additional output driver and said first processor unit and having the same structure as said input driver for reproducing said additional intercommunicating signals to supply the reproduced additional intercommunicating signals to said first processor unit.

10-17. (canceled)

18. (previously presented) The apparatus of claim 1, wherein,

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the intercommunicating signals from said first processor unit are operation mode signals comprising a signal ACTN representative of an active system, a signal SYNC representative of a duplex operation state, and a signal RUNN representative of an execution state.

19-20. (canceled)

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